

REMARKS

Claim 9 is amended to correct a typographical error. Claims 1-43 remain for consideration, and all claims are thought to be allowable over the cited art.

The objection to claims 33-43 as being substantial duplicates of claims 1-11 is respectfully traversed. Claim 1 includes "transmitting encrypted configuration data..." and independent claim 33 includes "receiving encrypted configuration data." Because "transmitting" is not identical to "receiving", the claims have different scope and are not substantially duplicative. For example, according to the Merriam-Webster Online Dictionary at <http://www.m-w.com>, "transmit" means "to send out (a signal) either by radio waves or over a wire", and "receive" means "to come into possession of", for example. Therefore, the claims are clearly different.

The Office Action does not establish that Claims 1-4, 12-16, 23-26, and 33-36 are anticipated by US patent publication number 2001/0037458 to Kean (hereinafter, "Kean") under 35 USC §102(e). The rejection is respectfully traversed because the Office Action fails to show that all the limitations of the claims are taught by Kean.

As to claims 1, 12, 23, and 33, for example, the Office Action does not show that Kean teaches the limitations of generating a fingerprint within the FPGA, the fingerprint representing an inherent manufacturing process characteristic that is unique to the FPGA. For example, one of the cited teachings of Kean shows creating wires in an FPGA with device artwork to connect to key input of the encryption circuit. Some point on each wire connects to power or ground to set a key bit. The key is defined by the connections of these wires to either power or ground. (para. #0134). Kean does not teach using a manufacturing process characteristic that is unique to the FPGA because it would be highly unlikely that a different wire pattern would be defined for each FPGA that is manufactured. Thus, Kean's wire patterns would not be unique to an FPGA. The

other cited sections of Kean are similarly lacking in teaching any use of a manufacturing process characteristic that is unique to the FPGA in generating a fingerprint.

Claims 2, 13, 24, and 34 depend from the independent claims discussed above and are allowable over Kean for at least the reasons set forth above.

As to claims 3, 14-16, 25-26, and 35, the Office Action alleges, but fails to show that the limitations of transmitting the fingerprint from the FPGA to an encryption circuit are taught by Kean. For example, Kean's FIG. 5 and paragraph #0055 clearly show Kean's improved secure FPGA encryption encompassing both a random number generator 72 and a security circuit 64. Thus, Kean does not transmit the key from the FPGA to the encryption circuit because Kean's random number generator and security circuit are part of the FPGA.

As to claims 4 and 36, Kean does not generate a fingerprint as explained above in regards to claims 1, 12, 23 and 33. Thus, Kean's power-up sequence would not involve generating the claimed fingerprint.

For at least the reasons set forth above, the Office Action fails to show that Kean anticipates claims 1-4, 12-16, 23-26, and 33-36.

The Office Action does not establish that claims 5, 9, 17, 19, 27, 28, 37 and 41 are unpatentable under 35 USC §103(a) over Kean in view of US patent number 5,838,256 to Pearson et al. (hereinafter, "Pearson"). The rejection is respectfully traversed because the Office Action fails to show that all the limitations are suggested by the references, fails to provide a proper motivation for modifying the teachings of Kean with teachings of Pearson, and fails to show that the combination could be made with a reasonable likelihood of success.

As to claims 5 and 37, the limitations include measuring propagation delays for a plurality of circuit elements on the FPGA, and combining the propagation delays to generate the fingerprint. The Office Action alleges that using propagation delays is well known in the art to generate a fingerprint. This

allegation is respectfully traversed because this is not thought to be well known. Furthermore, the Office Action does not provide any technical reasoning to support the allegation. Therefore the allegation is unsupported and should be withdrawn. Otherwise, a citation to prior art that shows this allegedly well known feature is respectfully requested so that the matter may be further addressed.

The cited portions of Pearson do not suggest the claim limitations. The cited portions (col. 17, l. 20 - col. 18) apparently teach nodes A and B that are driven by a totally symmetric cross-coupled pair of gates. The description further describes the behavior of Pearson's circuit when power is supplied. Nowhere is it apparent that Pearson measures any propagation delays and use the delays to generate the claimed fingerprint. Nor does the Office Action indicate any specific elements as meeting these limitations. Furthermore, the Office Action alleges that these portions of Pearson teach "measuring propagation delays and combining the propagation delays to generate signals to provide security to prevent attacker to crack the electronic key." However, Pearson does not describe, nor does the Office Action explain how, any propagation delays are actually measured and used in to prevent cracking of the electronic key. Since Pearson's teachings do not appear to support the interpretation alleged in the Office Action, further explanation is respectfully requested as to the specific elements of Pearson that are believed to support measuring the propagation delay and using the measurements to prevent cracking of the security key.

Claims 19 and 27 are apparatus claims, and to the extent that the limitations of claims 19 and 27 are similar to those of claim 5, the Office Action does not establish that the Kean-Pearson combination suggests the invention in claims 19 and 27.

The alleged motivation for modifying Kean with Pearson does not support *prima facie* obviousness. The alleged motivation simply states that it "would have been obvious because one skilled in the art would have been motivated by the suggestions

provided by Pearson et al. so as to provide security to prevent attacker to crack the electronic key." No further explanation is provided in the Office Action. This alleged motivation is insufficient because it is merely a broad, conclusory statement. There is no evidence provided to indicate which elements of the Kean could somehow be improved by specific elements of Pearson. The alleged motivation lacks clear and particular reasons that would lead one of ordinary skill in the art to combine specific teachings of Pearson with Kean.

Addressing the "rigorous ... requirement for a showing of the teaching or motivation to combine prior art references," the Court of Appeals for the Federal Circuit has stated:

We have noted that evidence of a suggestion, teaching, or motivation to combine may flow from the prior art references themselves, the knowledge of one of ordinary skill in the art, or, in some cases, from the nature of the problem to be solved, (citations omitted), although "the suggestion more often comes from the teachings of the pertinent references," *Rouffet*, 149 F.3d at 1355, 47 USPQ2d at 1456. The range of sources available, however, does not diminish the requirement for actual evidence. That is, the showing must be clear and particular. See, e.g., *C.R. Bard*, 157 F.3d at 1352, 48 USPQ2d at 1232. Broad conclusory statements regarding the teaching of multiple references, standing alone, are not "evidence." (citation omitted) *In re Dembiczak*, 175 F.3d 994, 50 U.S.P.Q.2d 1614 (Fed. Cir. 1999).

The alleged motivation is merely a broad conclusory statement of general applicability, and no evidence is provided to suggest the combination. Therefore, the alleged motivation is insufficient to support *prima facie* obviousness.

As to claims 9, 17, 28, and 41, the limitations include limitations related to determining line widths in the FPGA and using the line widths in generating the fingerprint. It is respectfully submitted that the cited portion of Pearson discusses transistor sizes, not line widths. Furthermore, there no indication that any size information is used in generating a fingerprint of an FPGA. Thus, the Office Action fails to show that the Kean-Pearson combination suggests the limitations of claims 9, 17, 28, and 41.

The rejection of claims 5,9,17,19,27,28,37 and 41 over the Kean-Pearson combination should be withdrawn because the Office Action fails to show all the limitations are suggested by the combination, fails to provide a proper motivation for combining the references, and fails to show that the combination could be made with a reasonable likelihood of success.

The Office Action does not establish that claims 6-8, 20-22, 30-32 and 38-40 are unpatentable under 35 USC §103(a) over Kean in view of US patent number 6,587,978 to Merrit et al. (hereinafter, "Merrit"). The rejection is respectfully traversed because the Office Action fails to show that all the limitations are suggested by the references, fails to provide a proper motivation for modifying the teachings of Kean with teachings of Merrit, and fails to show that the combination could be made with a reasonable likelihood of success.

Claims 6-8 and 38-40 include limitations of counting a number of oscillations of an oscillator in generating the fingerprint of the FPGA. The Office Action alleges that counting a number of oscillation is well known in the art to generate a fingerprint. This allegation is respectfully traversed because this is not thought to be well known. Furthermore, the Office Action does not provide any technical reasoning to support the allegation. Therefore the allegation is unsupported and should be withdrawn. Otherwise, a citation to prior art that shows this allegedly well known feature is respectfully requested so that the matter may be further addressed.

The Office Action is mistaken in the allegation that Merrit teaches using an oscillator to generate a fingerprint. Merrit's col. 4, ll. 22 - col. 5, ll. 16 apparently teaches using an oscillator and associated circuitry to enable testing of a DRAM having lockout circuitry (also, col. 2, ll. 34-35). Merrit's test key circuitry is used to control various test functions (col. 5, ll. 20-22). Merrit's oscillator serves to enable testing of the DRAM, not generate a fingerprint. Furthermore, there is no suggestion of generating a fingerprint that

represents an inherent manufacturing process characteristic unique to an FPGA.

Claims 20-22 are claims to an FPGA, claims 30-32 are apparatus claims, and to the extent that the limitations of claims 20-22 and 30-32 are similar to those of claims 6-8 and 38-40, the Office Action does not show that the Kean-Merrit suggests the inventions claimed in claims 20-22 and 30-32.

The alleged motivation for modifying Kean with Merrit does not support *prima facie* obviousness. The alleged motivation simply states that it "would have been obvious because one skilled in the art would have been motivated by the suggestions provided by Merrit et al. so as to reduce costs and save valuable manufacturing time." No further explanation is provided. Furthermore, this alleged motivation is insufficient because it is merely a broad, conclusory statement of an objective of all or nearly all chip manufacturing operations. There is no explanation given as to how manufacturing of Kean's FPGA is deficient and could be improved. Furthermore, there is no evidence provided to indicate which elements of the Kean could somehow be improved by specific elements of Merrit. The alleged motivation lacks clear and particular reasons that would lead one of ordinary skill in the art to combine specific teachings of Merrit with Kean. The alleged motivation is merely a broad conclusory statement of general applicability, and no evidence is provided to suggest the combination. Therefore, the alleged motivation is insufficient to support *prima facie* obviousness.

The rejection of claims 6-8, 20-22, 30-32 and 38-40 over the Kean-Merrit combination should be withdrawn because the Office Action fails to show all the limitations are suggested by the combination, fails to provide a proper motivation for combining the references, and fails to show that the combination could be made with a reasonable likelihood of success.

The Office Action does not establish that claims 10-11, 18, 29 and 42-43 are unpatentable under 35 USC §103(a) over Kean in view of US patent number 6,185,126 to Rogers et al.

(hereinafter, "Rogers"). The rejection is respectfully traversed because the Office Action fails to show that all the limitations are suggested by the references, fails to provide a proper motivation for modifying the teachings of Kean with teachings of Rogers, and fails to show that the combination could be made with a reasonable likelihood of success.

The Office Action fails to show that Rogers suggests the limitations of claims 10-11. Claims 10-11 and 42-43 include limitations of, among other limitations, using differences in transistor threshold voltages caused by manufacturing process variations to generate a fingerprint.

Rogers' teachings are for "setting the power-up state of some or all of the storage elements of a RAM-based FPGA or other programmable logic device to ensure that the proper state will be available immediately upon power up" (col. 1, l. 66 - col. 2, l. 3). Furthermore, the cited portion of Rogers teaches that the different threshold voltages of two transistors in a RAM cell are used to program a lookup table in the FPGA (col. 2, ll. 13-30). The claims make clear, and those skilled in the art will recognize that the claimed fingerprint is used to decrypt/encrypt the configuration data, and individual bits of the fingerprint are not used to program the FPGA as the Office Action seems interpret the claim limitations.

Claim 18 is a claim to an FPGA, and 29 is an apparatus claim. To the extent that the limitations of claims 18 and 29, the Office Action does not show that the Kean-Rogers combination suggests claims 18 and 29 for at least the reasons set forth above.

The alleged motivation for modifying Kean with Rogers does not support *prima facie* obviousness. The alleged motivation simply states that it "would have been obvious because one skilled in the art would have been motivated by the suggestions provided by Rogers et al. so as to eliminate the need for a separate programming operation following power-up." No further explanation is provided. Furthermore, this alleged motivation is insufficient because it is merely a broad, conclusory

statement and lacks clear and particular reasons that would lead one of ordinary skill in the art to combine specific teachings of Rogers with Kean. The alleged motivation is merely a broad conclusory statement of general applicability, and no evidence is provided to suggest the combination. Therefore, the alleged motivation is insufficient to support *prima facie* obviousness.

The rejection of claims 10-11, 18, 29 and 42-43 over the Kean-Rogers combination should be withdrawn because the Office Action fails to show all the limitations are suggested by the combination, fails to provide a proper motivation for combining the references, and fails to show that the combination could be made with a reasonable likelihood of success.

CONCLUSION

Reconsideration and a notice of allowance are respectfully requested in view of the Amendments and Remarks presented above. If the Examiner has any questions or concerns, a telephone call to the undersigned is invited.

Respectfully submitted,



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I hereby certify that this correspondence is being deposited with the United States Postal Service as first-class mail in an envelope addressed to: Commissioner for Patent, Washington, D.C. 20231, on September 2, 2004.

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